

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, NORIO MICHIE, a citizen of Japan residing at Tokyo, Japan, HIROMITSU SHIMIZU, a citizen of Japan residing at Kanagawa, Japan, YURIKO OBATA, a citizen of Japan residing at Tokyo, Japan, KIYOTAKA MOTEKI, a citizen of Japan residing at Tokyo, Japan, YASUHIRO HATTORI, a citizen of Japan residing at Kanagawa, Japan and TAKAO OKAMURA, a citizen of Japan residing at Tokyo, Japan have invented certain new and useful improvements in

DATA PROCESSING DEVICE CHARACTERIZED IN ITS DATA TRANSFER METHOD, PROGRAM FOR EXECUTING ON A COMPUTER TO PERFORM FUNCTIONS OF THE DEVICE, AND COMPUTER READABLE RECORDING MEDIUM STORING SUCH A PROGRAM

of which the following is a specification:-

**BACKGROUND OF THE INVENTION**

**1. Field of the Invention**

The present invention generally relates to a data processing device provided with a plurality of data processing units, wherein each data processing unit makes an access to a memory shared for data storage so as to perform an operation.

The present invention further relates to an image-forming device, which image-forming device can efficiently perform input/output operations of image signals of a digital copying machine, a facsimile, a printer, etc.

**2. Description of the Related Art**

Recently and continuing, the digitization of copying machines, etc., is in progress. Based on this progress, many image processing functions other than processing and editing images are becoming incorporated in the copying machines.

An example of such image processing functions is an electronic sorting function, which can dispense with the manual sorting operation by storing image data of a plurality of manuscripts in a memory and by providing a designated number of copies of manuscripts all at once. However, when the image data of the

manuscripts is to be stored in the memory, the cost of the memory becomes high since the amount of image data is enormous. Accordingly, in order to reduce the memory cost, the following configurations are generally used.

- 5     1. First configuration - A semiconductor memory and a storage memory. A secondary storage device such as a hard disk device, which is less expensive than the semiconductor memory, is used as the storage memory (secondary memory).
- 10    2. Second configuration - A semiconductor memory is used as the storage memory. By reducing the data amount per image through image data compression operations, the necessary memory capacity is reduced.
- 15    3. Third configuration - A single memory is shared by a plurality of image input/output means (for example, an image scanner, a printer controller, a file server, and a facsimile controller).

For executing image input/output operations with respect to the memory, a memory controller (DMA controller) that uses a Direct Memory Access (DMA) data transfer method is often used. (See, for example, Japanese Laid-Open Patent Application No. 6-103225 and NO. 2000-158724.) The DMA controller performs access/data transfer with respect to a particular region of the memory based on memory region management

information referred to as a descriptor, which management information indicates the procedure for the data transfer. It is also possible to perform the data transfer by dividing the memory region into which a 5 single image is stored by a plurality of descriptors. For example, the memory may be used in the form of a ring buffer so as to execute input/output of the image data using less memory capacity as compared to the image data amount.

10           The memory access control using the DMA controller enables the system to keep track of current status of the data transfer (start and finish) designated by each descriptor and to control the execution timing of the data transfer (interruption or 15 resumption of data transfer when accessing the image memory regions and interruption completion report of each descriptor, etc.). Accordingly, there are advantages such as high flexibility of timing control of access/data transfer with respect to the memories such 20 as a semiconductor memory and a large-capacity secondary memory device, which are connected to the DMA controller, and a broad scope of application.

              In the above-mentioned first configuration, generally, a plurality of data transfer operations (data 25 writing operation and data reading operation) cannot be

performed simultaneously with respect to a single memory device. Therefore, it is common to divide the data transfer (access) unit with respect to the secondary memory device by descriptors of the DMA controller. This  
5 is done in a time-multiplexed way so that it looks as if the plurality of data transfer operations are performed in parallel.

However, when such a time-multiplexed process is used, the overall amount of time needed for the data  
10 transfer is not reduced. Accordingly, in devices such as an image-forming device, in which the reduction in the amount of time needed for the input/output of image data has influence on the device productivity, the use of a time-multiplexed process may reduce the device  
15 productivity. Accordingly, in such an image-forming device, the above-mentioned second configuration may be employed, or a secondary memory device with a rapid data transfer rate may be implemented so as to reduce the time needed for the data transfer to the secondary  
20 memory device.

Further, in the image-forming device according to the related art, for the reason of simplifying the memory control, the time-multiplexed transfer is not preferably performed. Instead, in general, the  
25 secondary memory device is used as a resource and

performs the data transfer approximately in phase with the image data input/output operation by the image input/output means.

In general, when compared with a first data transfer rate between the image input/output means and the semiconductor memory, a second data transfer rate between the semiconductor memory and the secondary memory device is low. The difference between the first data transfer rate and the second data transfer rate does not change even when the amount of data to be transferred to the secondary memory device is reduced by image compression. Therefore, the productivity of the image-forming device does not improve significantly even when the transferring timing of the data transfer process (including data conversion processes such as data compression, etc.) between the semiconductor memory and the secondary memory device is independently and appropriately controlled.

The transfer rate of the secondary memory device such as a hard disk device is improving year by year, and such improvement has also enabled an increasing productivity of the image-forming devices. However, a recent high-speed machine requires an even higher data transfer rate since such a machine reads both sides of the manuscript simultaneously; the

processing ability (processing speed) of the image input/output means is improved; and further there are some machines with a mechanical constraint in that predetermined productivity cannot be realized unless the  
5 manuscript feeding process is performed in the non-interval mode. Accordingly, these days, the current data transfer (access) status with respect to the secondary memory device and the characteristics thereof, etc. are taken into consideration for switching between  
10 interval control and non-interval control of manuscript feeding.

Accordingly, with the recent improvements in devices such as an image-forming device as mentioned above, the data transfer rate with respect to the  
15 secondary memory device with large capacity such as a hard disk device, etc., is not always sufficient when compared with the data transfer rate with respect to the image input/output means even when the amount of data is reduced by data compression.

20 As an example, when image output means is to provide a color image from image data with multiple colors, the color image cannot be properly provided unless the image data stored in the secondary memory device is provided within a predetermined period of time,  
25 or the productivity of the device is significantly

reduced since the time needed for providing the color image is long. Therefore, it is necessary for the image-forming device to cope with such a problem.

As another example, when a device such as an 5 image-forming device is provided with a facsimile function, the facsimile transmission may be placed under restraint related to the data transfer time period in the protocol for data transfer using telephone lines. Accordingly, unless the data transmission is performed 10 within a certain period of time, the connection is cut and thus the data cannot be transmitted. This facsimile transmission function is a typical function in such a device. Therefore, it is necessary for the image-forming device to cope with such a problem.

15 Further, when a device such as an image-forming device can perform a plurality of image signal input/outputs in parallel simultaneously, the efficiency of the image signal processing (input: storage, output: reading out) with respect to the secondary memory device 20 becomes a key factor for improving the productivity of the image-forming device. However, under the current circumstances where there is a wide variety of image input/output means, it is becoming more challenging for the image-forming device to assure high productivity by 25 maximally utilizing the memory device and capability of

the data compression means.

SUMMARY OF THE INVENTION

Accordingly, it is a general object of the  
5 present invention to provide a data processing device  
that comprises a plurality of data processing units,  
wherein, the data processing unit makes an access to a  
memory shared for data storage including a secondary  
memory device so as to meet a constraint of data  
10 transfer time when at least one of the data processing  
units having such a constraint.  
15

It is another object of the present invention  
to provide an image-forming device with high  
productivity, which image-forming device is capable of  
15 efficiently controlling the data transfers in accordance  
with the processing capability of the memory device by  
using the Direct Memory Access (DMA) data transfer  
method.

It is another object of the present invention  
20 to provide an image-forming device, which image-forming  
device is capable of performing optimal image  
input/output operations in accordance with the image  
signal transfer rate between image input/output means  
and the memory device, which rate is determined from the  
25 processing time constraint and configuration of the

image input/output means and their peripheral control devices.

As a first aspect of the present invention, there is provided a data processing device comprising a plurality of data processing units; a first memory shared for storing data, to which first memory each of the data processing units makes an access so as to perform an operation; a transfer completion time designation unit for designating a transfer completion time according to need, within which transfer completion time, transferring the data in response to the accesses made by the data processing units should be completed; an expected transfer completion time calculation unit for calculating an expected transfer completion time needed for completing the data transfer in response to the accesses made by the data processing units, the expected transfer completion time calculation unit calculating the expected transfer completion time by taking current access status of the first memory into consideration; and an access management unit for managing the access to the first memory based on the transfer completion time and the expected transfer completion time.

Accordingly, since the data processing device according to the present invention executes the data

transfers in response to the accesses by taking the current access status of the memory into consideration, it is possible to execute the data transfer so as to meet a constraint related to the time needed for the  
5 data transfer, if any.

In the data processing device according to the present invention, the device may further comprise a second memory for storing the data stored in the first memory, which second memory having a transfer rate lower  
10 than the transfer rate of the first memory, and when the data transfer is executed between the first memory and the second memory, the expected transfer completion time calculation unit may calculate the expected transfer completion time by taking the data transfer rates of the  
15 first memory and the second memory into consideration.

Accordingly, since the data processing device according to the present invention executes the data transfers in response to the accesses by taking the data transfer rates of the first memory and the second memory into consideration, it is possible to execute the data transfer so as to meet a constraint related to the time needed for the data transfer, if any.  
20

In the data processing device according to the present invention, when one of the data processing units  
25 makes an additional access to the first memory, the

access management unit may prevent or postpone the additional access to the first memory when the expected transfer completion time exceeds the transfer completion time.

5           Accordingly, since the additional access and its accompanying data transfer is prevented or postponed when the expected transfer completion time exceeds the transfer completion time, it is possible to provide a data processing device that executes the data transfers  
10       so as to meet a constraint related to the time needed for the data transfer, if any.

The data processing device according to the present invention may be an image-forming device provided with one data processing unit as an image input  
15       unit for inputting image data to the first memory and one data processing unit as an image output unit for outputting the image data stored in the first memory.

Therefore, in the data processing device according to the present invention, the accessing by the  
20       data processing units of the memory is managed based on the transfer completion time designated by the transfer completion time designation unit, within which transfer completion time, transferring the data in response to the accesses made by the data processing units should be  
25       completed; and the expected transfer completion time

calculated by the expected transfer completion time calculation unit, which expected transfer completion time is needed for completing the data transfer in response to the accesses made by the data processing units, the expected transfer completion time calculation unit calculating the expected transfer completion time by taking current access status of the first memory into consideration. Thus, with the data processing device according to the present invention, even when there is constraint related to the time needed for transferring the data, it is always possible to make an access to the memory and perform data transfer in response to such an access so as to meet such constraint.

As a result, each of the data processing units provided to the data processing device according to the present invention can always optimally perform its process without substantially decreasing the processing rate and therefore, high productivity of the data processing device can be maintained.

To put it differently, when accesses are made to the memory by the data processing units so as to perform operations, the expected transfer completion time is calculated based on the data transfer processes corresponding to the accesses made. When the expected transfer completion time exceeds the allowable transfer

completion time, some of data transfer processes  
(usually data transfer processes that are requested at a  
later time than others) are prevented or postponed.  
Since some of the data transfer processes are prevented  
5 or postponed so as not decrease the processing rates of  
respective data processing units, it is always possible  
to execute only the data transfer processes that can be  
actually completed within the allowable transfer  
completion time. The productivity of the data  
10 processing device according to the present invention can  
be improved since some of the data transfer processes  
are prevented or postponed before the actual operations  
of the data processing units, which requested such data  
transfer processes, are started, and accordingly since  
15 execution of wasteful data transfer processes, which are  
to be disabled due to their impossibility of  
completing the data transfer processes within the  
allowable transfer completion time, is prevented.

In addition, according to the present  
20 invention, there is provided a program for executing on  
a computer to perform the functions of a plurality of  
data processing units; a first memory shared for storing  
data, to which first memory each of the data processing  
units makes an access so as to perform an operation; a  
25 transfer completion time designation unit for

designating a transfer completion time according to need,  
within which transfer completion time, transferring the  
data in response to the accesses made by the data  
processing units should be completed; an expected  
5 transfer completion time calculation unit for  
calculating an expected transfer completion time needed  
for completing the data transfer in response to the  
accesses made by the data processing units, the expected  
transfer completion time calculation unit calculating  
10 the expected transfer completion time by taking current  
access status of the first memory into consideration;  
and an access management unit for managing the access to  
the first memory based on the transfer completion time  
and the expected transfer completion time.

15 Further, according to the present invention,  
there is provided a computer-readable recording medium  
storing a program for executing on a computer to perform  
the functions of a plurality of data processing units; a  
first memory shared for storing data, to which first  
20 memory each of the data processing units makes an access  
so as to perform an operation; a transfer completion  
time designation unit for designating a transfer  
completion time according to need, within which transfer  
completion time, transferring the data in response to  
25 the accesses made by the data processing units should be

completed; an expected transfer completion time calculation unit for calculating an expected transfer completion time needed for completing the data transfer in response to the accesses made by the data processing units, the expected transfer completion time calculation unit calculating the expected transfer completion time by taking current access status of the first memory into consideration; and an access management unit for managing the access to the first memory based on the transfer completion time and the expected transfer completion time.

As a second aspect of the present invention, there is provided an image-forming device comprising an image input unit; an image output unit; a storage unit for storing an image signal provided from the image input unit in a primary storage part, and for storing the image signal stored on the primary storage part in a secondary storage part; a delivering unit for delivering the image signal stored in the primary storage part, which image signal is read out from the secondary storage part, to the image output unit; and a priority designation unit for designating priority for each of a plurality of image signal input/output operation requests.

Since priority for each of the image signal

input/output operation requests can be designated, it is possible to efficiently execute a series of image signal input/output operations based on the priority.

Therefore, the image signal input/output operations can  
5 be efficiently controlled according to the processing capability of the memory device. Accordingly, an image-forming device, which is capable of efficiently controlling the data transfers in accordance with the processing capability of the memory device, can be  
10 provided.

The image-forming device according to the present invention may further comprise a request acceptance unit for accepting the image signal input/output operation requests; a processing order control unit for determining a processing order of the image signal input/output operation requests based on respective priorities designated by the priority designation unit; and an interruption/resumption control unit for interrupting a current image signal  
15 input/output operation request when the priority of the current image signal input/output operation request is lower than the highest priority of an image signal input/output operation request among the image signal input/output operation requests, and for resuming the  
20 current image signal input/output operation request  
25

after completion of the image signal input/output operation request with the highest priority.

In the image-forming device according to the present invention, the image signal input/output operation request with the highest priority is extracted from the image signal input/output operation requests, each of which is provided with a priority. When the priority of the image signal input/output operation request with the highest priority among the image signal input/output operation requests is higher than the priority of the current image signal input/output operation request, and when such a current image signal input/output operation request is interruptible, the operation of the current image signal input/output operation request is interrupted; the operation of the image signal input/output operation request with the higher priority is executed; and the operation of the interrupted image signal input/output operation request is resumed when the operation of the image signal input/output operation request with higher priority is completed. Accordingly, the processing time needed for the operation of the image signal input/output operation request with higher priority can be reduced. Therefore, an image-forming device, which is capable of efficiently controlling the data transfers in accordance with the

processing capability of the memory device, can be provided.

It is noted that there may be also provided a designation unit for designating interruptibility or  
5 non-interruptibility of the operation of the current image signal input/output operation request.

The image-forming device according to the present invention may further comprise a selection unit for selectively executing the control of the processing  
10 order control unit and the interruption/resumption control unit.

Accordingly, it is possible to employ the processing order control based on priority according to need. Therefore, an image-forming device, which is  
15 capable of performing optimal image input/output operations, can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a data  
20 processing device (an image-forming device) according to the invention;

FIG. 2 is a diagram for illustrating the scanning of an image of a manuscript provided on a manuscript table;

25 FIG. 3 is a timing chart for illustrating the

outputting of image data by an image processor unit (IPU) in a reading unit;

FIG. 4 is a schematic diagram of a storage unit;

5 FIG. 5 is a schematic interior diagram of a memory control part in the storage unit;

FIG. 6 is a diagram for illustrating an access operation (data transfer operation) by a descriptor of an image input/output direct-memory-access controller  
10 (DMAC);

FIG. 7 shows two tables illustrating waiting queues managed by a system control unit;

FIG. 8 is a flow chart illustrating processing operation of priority designation means;

15 FIG. 9 is a flow chart illustrating processing operation of processing order control means and interruption/resumption control means;

FIG. 10 is a flow chart illustrating processing operation of input/output operation request  
20 acceptance means accepting a plurality of image signal input/output operation requests;

FIG. 11 is a flow chart illustrating a processing operation of transferring of data in a primary memory region to a secondary memory region in a  
25 single transfer;

FIG. 12 is a flow chart illustrating a processing operation of transferring of the data in the primary memory region to the secondary memory region in multiple transfers;

5 FIG. 13 is a flow chart illustrating a processing operation of interruption designation means; and

10 FIG. 14 is a flow chart illustrating a processing operation of priority based processing selection means.

**DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

In the following, principles and embodiments of the present invention are described with reference to 15 the accompanying drawings.

A first embodiment according to the present invention is described below.

FIG. 1 is a schematic diagram of a data processing device according to the present invention. 20 Here, a digital copying machine is shown as an example of the data processing device; however, the present invention is not limited thereto.

As shown in FIG. 1, the digital copying machine according to the present invention is provided 25 with a reading unit 1 for reading an image of a

manuscript, an image-forming unit 2 for forming  
(printing) the image on a transfer medium, a storage  
unit 3 for storing the image data, an operational unit 4  
arranged with various keys and a display, and a system  
5 control unit 5 for controlling each part of the device  
based on operational information from the operational  
unit 4. Further, a facsimile unit 6 for receiving and  
transmitting data through telephone lines is switchably  
connected via a selector unit 7 for switching  
10 destinations of the image data.

The reading unit 1 performs scan exposure on a  
manuscript A by displacing an exposure lamp 12 along the  
manuscript table 11 in the sub-scanning direction as  
shown in FIG. 2. The reflected light is directed to a  
15 CCD image sensor 13 by a plurality of reflectors. The  
image sensor 13 performs photoelectric conversion and  
generates electric signals according to the strength of  
the reflected light. An image-processing unit (IPU) 14  
generates digital image data of 8 bits with respect to  
20 the electric signals by performing analog-to-digital  
conversion after shading correction, etc.

The IPU 14 further performs image processes such as  
magnification change, dithering, etc. If the image data  
after the image processes is to be output immediately,  
25 the image data is provided to the image-forming unit 2

with an image synchronization signal.

A scanner control part 15 processes detected data from various sensors and controls a drive motor for displacing the exposure lamp 12, etc., and further

5 performs setting of various parameters for the IPU 14 in order to realize the above-mentioned processes.  
Accordingly, the scanner control part 15 performs the overall control of the reading unit 1.

Now referring to FIG. 3, an image data output  
10 of the IPU 14 of the reading unit 1 is described below.

A frame gate signal /FGATE is a signal indicating an image effective range of the image area in the sub-scanning direction. When the signal /FGATE is low level (low active), the image data is available.

15 The signal /FGATE is either asserted or negated by a falling edge of a line synchronization signal /LSYNC. The signal /LSYNC is asserted by a rising edge of a pixel synchronization signal PCLK for a predetermined number of clocks. The image data in the main-scanning  
20 direction is available after the rising edge of the signal PCLK and after the predetermined number of clocks. One image data set is provided with respect to one cycle of the signals PCLK and corresponds to the division in the main-scanning direction into approximately 157.5 DPC  
25 (=4,000 DPI). The image data set is delivered in the

raster format, in which format, the image data in the main-scanning direction is provided as the position in the sub-scanning direction is changed. The effective range in the sub-scanning direction is generally defined  
5 by the size of the transfer medium.

Referring to FIG. 1 again, in the image-forming unit 2, the image data is provided to a writing part 16 and a photoconductor 18 rotating at constant velocity and uniformly charged by an electric charger 17  
10 is exposed to laser light modulated according to the image data from the writing part 16. An electrostatic latent image is formed on the photoconductor 18 by being exposed to such laser light and a toner image is formed by being developed by a developing part 19. The  
15 transfer medium in a feeding tray 21 is conveyed to a pair of resist rollers 22 by a pair of feeding rollers 20. The feeding of the transfer medium by the resist rollers 22 is started at timing when the toner image on the photoconductor overlaps the transfer medium. A  
20 transfer charger 23 electrostatically transfers the toner image from the photoconductor 18 onto the transfer medium. The part of the transfer medium onto which part the toner image is transferred is separated from the photoconductor 18 by a separation charger 24. The toner  
25 image on the transfer medium is thermally fixed by a

fixing part 25, after which the transfer medium is delivered to a delivery tray by a pair of delivery rollers 26.

The toner remaining on the photoconductor 18  
5 after the electrostatic transfer is cleaned by a cleaner part 27. After cleansing, the photoconductor 18 is electrically discharged by an electric discharger 28. A plotter control part 29 processes detected data from various sensors and controls various drive motors for  
10 the driving photoconductor 18, the pair of feeding rollers 20, the pair of resist rollers 22, the fixing part 25, etc.

The system control unit 5 performs, through transmission, setting of various parameters, process  
15 execution indications, etc., for the reading unit 1, the storage unit 3, the image-forming unit 2, and the facsimile unit 6 in response to the operations performed by a user on the operational unit 4. The status of the overall device is displayed on the display of the  
20 operational unit 4. Accordingly, the system control unit 5 performs the overall control in response to the operations performed by the user on the operational unit 4.

The facsimile unit 6 performs, according to  
25 the indications from the system control unit 5, digital

image data compression with respect to the image data provided from the IPU 14 or the storage unit 3 based on G3, G4 facsimile data transfer standards and transfers the compressed image data to the telephone line. On 5 receiving data from the telephone line, the facsimile unit 6 restores the data and provides the restored data to the writing part 16 of the image-forming unit 2, etc., and the received data is made visible.

The selector unit 7 changes the connection 10 status of its selector depending on the indications from the system control unit 5 and selects one from the reading unit 1, the storage unit 3, and the facsimile unit 6 as the output destination of the image data.

The storage unit 3 is generally used for 15 duplication applications such as repeat copying, rotation copying, etc., by storing the image data of the manuscript provided from the IPU 14. The storage unit 3 may also be used as a buffer memory for temporarily storing the digital image data from the facsimile unit 6. 20 The storage of the data is performed as indicated by the system control unit 5.

FIG. 4 is a schematic diagram of the storage unit 3.

An image input/output direct memory access 25 controller (DMAC) 31 consists of a central processing

unit (CPU) and a logic circuit, and performs transmission with a memory control part 33 so as to receive commands. The image input/output DMAC 31 performs operation setting responsive to the commands.

5 The memory control part 33 is provided with status information indicating the current status of the image input/output DMAC 31.

On receiving the image input command from the memory control part 33, the image input/output DMAC 31

10 packs the image data provided by way of the selector unit 7 into memory data in units of 8 pixels according to the image synchronization signal /FGATE, and provides it to the memory control part 33 as needed with the memory access signal. On receiving the image output

15 command, the image input/output DMAC 31 provides the image data received from the memory control part 33 in phase with the image synchronization signal /FGATE.

An image memory 32 is where the image data is stored and consists of a semiconductor memory element

20 such as DRAM, etc. The memory capacity of the image memory is, for example, 157.5 DPC (=4,000 DPI) corresponding to 8 megabytes (MB), which is the sum of 4 MB for A3 size and 4 MB for electronic sorting storage, both with respect to binary image data. The image

25 memory 32 is accessed by the memory control part 33.

The memory control part 33 consists of a CPU and a logic circuit, performs transmission with the system control unit 5 so as to receive commands, performs operation setting responsive to the commands, 5 and provides status information indicating the current status of the storage unit 3 to the system control unit 5.

The commands from the system control unit 5 include commands indicating image input, image output, 10 compression, decompression, etc., and the image input commands and the image output commands are provided to the image input/output DMAC 31 and the commands related to compression are provided to an image transfer DMAC 36, a code transfer DMAC 37, and a compression-decompression 15 part 38.

FIG. 5 is a schematic interior diagram of the memory control part 33. The interior configuration and operation of each part is described below with reference to FIG. 5.

20 An input/output image address counter 33a counts up input/output memory access request signals provided from the image input/output DMAC 31, and provides memory address data of 22 bits indicating the storage location where the input/output image data is 25 stored. At the beginning of memory access, the address

is initialized once.

A transfer image address counter 33b counts up transfer memory access enable signals provided from an arbiter 33g, and provides memory address data of 22 bits 5 indicating the storage location where the transfer image data is stored. At the beginning of memory access, the address is initialized once.

A difference calculation part 33c calculates, at the time of image data input, the difference between 10 the input/output process line number provided from the image input/output DMAC 31 and the transfer process line number provided from the compression-decompression part 38. The obtained difference (difference line number) is provided to a difference comparison part 33d.

15 The difference comparison part 33d compares, at the time of image data input, the difference line number provided from the difference calculation part 33c and a set value provided from a line setting part 33e. When the difference line number is equal to the set 20 value, then the difference comparison part 33d provides an inactive transfer request mask signal to a request mask 33f and when the difference line number is not equal to the set value, then the difference comparison part 33d provides an active transfer request mask signal 25 to the request mask 33f. Other than the above or when

input/output of image data is not being performed, the signal is made inactive.

The line setting part 33e sets, when the image memory part 32 is used as a buffer at the time of image data input, the set value to be used for the comparison in the difference comparison part 33d based on a setting request from the system control part 5. Any value can be set.

The request mask 33f masks (i.e. puts in a disabled status) the transfer memory access request signal for allowing the compression-decompression part 38 to access an HDD 34 via an HDDC 35 (see FIG. 4) according to the transfer request mask signal from the difference comparison part 33d, and stops the data transfer process.

The arbiter 33g provides the transfer memory access enable signal indicating that the compression-decompression part 38 can access the HDD 34. Such a signal is provided based on the input/output memory access signal from the image input/output DMAC 31 and the transfer memory access request signal provided by way of the request mask 33f.

An address selector 33h selects one from the address data from the input/output image address counter 33a and the address data from the transfer image address

counter 33b according to the arbiter 33g.

An access control circuit 33i distributes the address data provided by way of the address selector 33h into row addresses and column addresses, and provides it 5 to an address bus of 11 bits. In addition, according to an access start signal from the arbiter 33g, the access control circuit 33i provides a control signal (RAS, CAS, WE) for the image memory 32.

In the above configuration of the image  
10 control part 33, the image input indication from the system control unit 5 initializes the memory control part 33 and puts the memory control part 33 in a waiting status for image data, and the image data can be stored in the storage unit 3 through operation of the reading  
15 unit 1. The image data provided to the storage unit 3 is temporarily written in the image memory 32. The number of process lines of the written image data is counted in the image input/output DMAC 31 and the counted number is transmitted to the memory control part  
20 33 as the input/output process line number. The compression-decompression part 38 receives the image transfer command from the memory control part 33 and provides the transfer memory access request signal thereto; however, the transfer memory access request  
25 signal is masked by the request mask 33f of the memory

control part 33 and thus access due to such a signal is not performed. When one line of the image data from the image input/output DMAC 31 is completed, the masking of the transfer memory access request signal is released; 5 the reading out of the image data from the image memory 32 is performed; and the transfer operation of the compression-decompression part 38 is started. During such operation, the difference between the two process line numbers is calculated in the difference calculation 10 part 33d and when the difference is equals to 0, the transfer memory access request signal is masked to ensure that there is no passing of address.

Now referring to FIG. 4 again, further details of the storage unit 3 are given below.

15           The image transfer DMAC 36 consists of a CPU and a logic circuit, performs transmission with the memory control part 33 so as to receive commands, performs operation setting responsive to the commands, and provides status information indicating the current 20 status to the memory control part 33. On receiving a compression command, the image transfer DMAC 36 provides the memory access request signal to the memory control part 33 and receives the image data when the memory access enable signal is active, and the image data is 25 transferred to the compression-decompression part 38.

The image transfer DMAC 36 houses an address counter that counts up the memory access request signals. The image transfer DMAC 36 provides memory address data of 22 bits for reading out the image data or for indicating 5 the storage location where the image data is stored, which memory address data is generated using the counted value.

The code transfer DMAC 37 consists of a CPU and a logic circuit, performs transmission with the 10 memory control part 33 so as to receive commands, performs operation setting responsive to the commands, and provides status information indicating the current status to the memory control part 33. On receiving a decompression command, the code transfer DMAC 37 15 provides the memory access request signal to the memory control part 33 and receives the image data when the memory access enable signal provided from the memory control part 33 is active, and the image data is transferred to the compression-decompression part 38.

20 The code transfer DMAC 37 houses an address counter that counts up the memory access request signals. The code transfer DMAC 37 provides memory address data of 22 bits for reading out the image data or for indicating the storage location where the image data is stored, which 25 memory address data is generated using the counted value.

The compression-decompression part 38 consists of a CPU and a logic circuit, performs transmission with the memory control part 33 so as to receive commands, performs operation setting responsive to the commands, 5 and provides status information indicating the current status to the memory control part 33. The compression-decompression part 38 compresses the binary image data with the MH coding method.

The HDD controller (HDDC) 35 consists of a CPU 10 and a logic circuit, performs transmission with the memory control part 33 so as to receive commands, performs operation setting responsive to the commands, and provides status information indicating the current status to the memory control part 33. The HDDC 35 15 performs the reading out or accessing (data transfer) of the status information of the HDD 34. The HDD 34 is the secondary memory device.

The storage unit 3 with the above-mentioned configuration, at the time of image input and data 20 storage, writes the image data in the storage region reserved in the image memory 32 by the image input/output DMAC 31, or reads out the image data stored in the storage region though the indication from the system control unit 5. At this time, the image 25 input/output DMAC 31 counts the number of lines of the

image data and provides the counted number as the input/output process line number to the memory control part 33.

FIG. 6 is a diagram for illustrating the  
5 accessing operation (data transfer operation) by the descriptor of the image input/out DMAC 31. In this example, the image data is divided into 4 bands and the data transfer is carried out with respect to such image data. It is noted that the operations in other DMACs  
10 such as DMAC 36 and DMAC 37 are the same as that of the DMAC 31.

First, the process of adding the total transfer line number (number of lines to be transferred) in a single image data is described.

15 When the image input/output DMAC 31 receives the transfer command from the memory control part 33, a descriptor storage register 31a inside the image input/output DMAC 31 is loaded with the contents of the descriptor 1 in the memory by accessing a chain  
20 destination address (a-address) set by the CPU. The loaded contents are constructed from 4 words including the chain destination address (head address) indicating the storage region of the next descriptor, a data transfer destination address indicating the head address  
25 of transferring data, a data transfer line number

indicating the amount of data to be transferred in line numbers, and format information designating whether a CPU interrupt is to be generated when the data transfer of the set line number is completed. The least  
5 significant bit of the format information is provided for designating whether the CPU interrupt is to be generated when the data transfer of the set line number is completed. When the value of the bit is 0, the CPU interrupt is generated and when the value of the bit is  
10 1, the CPU interrupt is not generated.

In the example shown in FIG. 6, the image data is divided into 4 bands and the value of the least significant bit of the format information of each descriptor is set to 0. Therefore, when the image  
15 transfer of each band is completed, a CPU interrupt is generated. Due to such CPU interrupts, it is possible to perform data transfer while detecting the transfer completion timing and the line numbers by adding the line numbers set to each descriptor.

20 When transferring the image data from the image memory 32 to the HDD 34 via the compression-decompression part 38 (i.e. when transferring the image data from the primary memory device to the secondary memory device), since the setting of the descriptor of  
25 the memory control part 33 is for data transfer of one

band, the setting of the line number of the descriptor is set as the image line number. The descriptor storing such a line number and having the storage destination address indicating the code transfer DMAC 37 is provided

5 to the image transfer DMAC 36. In the descriptor having the storage destination address indicating the code transfer DMAC 37, the data storage destination address is set to the HDDC 35. Accordingly, the image data transfer in the following path is realized. That is to

10 say, image memory 32 → memory control part 33 → image transfer DMAC 36 → code transfer DMAC 37 → compression-decompression part 38 → HDDC 35 → HDD 34. After the completion of the data transfer, the HDDC 35 reports the capacity used when storing the data into the HDD 34.

15 The storage address (for example, the head address) indicating where the image data is stored in the HDD 34 and the used capacity is stored in an HDD management region reserved in the image memory (the primary memory device) 32. During the data transfer, the memory

20 control part 33 masks the transfer memory access request so that the image data transfer to the compression-decompression part 38 does not get ahead of the image data transfer from the image input/output DMAC 31 (i.e., the data transfer to the secondary memory device is

25 controlled so as not to get ahead of the data transfer

of the image input).

On the other hand, when transferring the image data from the HDD 34 to the image memory 32 via the compression-decompression part 38 (i.e. when

5 transferring the data from the secondary memory device to the primary memory device), the storage address and the used capacity stored in the HDD management region reserved in the image memory 32 are obtained. The storage destination address is designated for the HDDC

10 35, the used capacity is designated for the code transfer DMAC 37, and the line number after decompression is designated for the image transfer DMAC 36. Then, the image transfer is performed in the following path. That is to say, HDD 34 → HDDC 35 →

15 compression-decompression part 38 → code transfer DMAC 37 → image transfer DMAC 36 → memory control part 33 → image memory 32. When performing data transfer in paths other than the mentioned paths, the memory control part 33 provides the descriptor created in a similar way to

20 any DMAC so as to realize the data transfer in the paths other than the mentioned paths.

Accordingly, the image memory 32 and the HDD 34 are shared for storage of the image data to be processed. According to the first embodiment of the

25 present invention, conventional problems such that each

of the reading unit 1, the image-forming unit 2, and the facsimile unit 6 cannot properly perform respective processes and the time needed for such processes becomes unacceptably long, which problems arise due to the  
5 decrease in the data transfer rate caused by such sharing, are prevented as described below.

The data transfer rate changes according to the system configuration and employed devices. In the first embodiment according to the present invention, the  
10 data transfer rate (rx\_speed1) from the reading unit 1 (facsimile unit 6) to the image memory 32; the data transfer rate (rx\_speed2) from the image memory 32 to the HDD 34, all above at the time of data input; the data transfer rate (tx\_speed1) from the HDD 34 to the  
15 image memory 32; and the data transfer rate (tx\_speed2) from the image memory 32 to the image-forming unit 2 (facsimile unit 6), etc. are previously stored on a non-volatile memory (not shown) comprised in the system control unit 5, as inherent characteristic values.

20 An expected transfer completion time (expect\_time), which is the time when the data transfer is expected to be completed, is calculated by taking the amount of data (data1); the path of the data transfer; and the data transfer rate determined from the path into  
25 consideration.

For example, when the image data provided from the reading unit 1 is to be stored on the HDD 34, the expected transfer completion time is calculated as follows:

5    expect\_time=data1/rx\_speed1+data1/rx\_speed2+wait\_time

For example, when the image stored on the HDD 34 is to be provided to the image-forming unit 2, the expected transfer completion time is calculated as follows:

10    expect\_time=data1/tx\_speed1+data1/tx\_speed2+wait\_time

wherein, wait\_time is the waiting time actually needed for processes other than the data transfer. The waiting time varies depending on the current operational status as shown below.

15    wait\_time=WAIT\_DRAM+WAIT\_HDD+α

wherein, **WAIT\_DRAM** is the time necessary until the image memory 32 becomes available for the relevant request by being released from other requests, which are in advance occupying the image memory 32. **WAIT\_DRAM** is calculated taking remaining time of the expected transfer completion time of the current transfer request; the presence of other transfer requests, which are currently waiting; and the expected transfer completion time of other transfer requests, if such requests are present, into consideration. **WAIT-HDD** is the time necessary

until the HDD 34 becomes available for the relevant request by being released from other transfer requests, which are in advance occupying the HDD 34. WAIT\_HDD is calculated in a similar way as WAIT\_DRAM.  $\alpha$  is the time 5 needed for overhead other than mentioned above, and the worst value (the longest value) is used as a fixed value.

The waiting time (wait\_time) is obtained, for example, by the memory control part 33 calculating WAIT\_DRAM and WAIT-HDD, and is then reported to the 10 system control unit 5. Then the system control unit 5 calculates the expected transfer completion time (expect\_time) using the waiting time reported by the memory control part 33. The amount of data (data1) necessary for calculating the waiting time is obtained 15 from the request origin, which requested the data transfer.

The system control unit 5 designates, at the time of data transfer request, a transfer completion time (complete\_time), which is the time when the data 20 transfer is to be completed, according to need. The transfer completion time is calculated based on the amount of data and the lowest data transfer rate needed at the data transfer designation or the data transfer origin. By comparing the transfer completion time 25 (complete\_time) and the expected transfer completion

time (expect\_time), it is determined whether the actual data transfer completes within the transfer completion time.

When the data transfer is performed in the  
5 time-multiplexed process, the expected transfer completion times of other transfer requests may change by performing the requested data transfer. Accordingly, when it is determined that the data transfer completes within the transfer completion time, the expected  
10 transfer completion time when an additional data transfer is requested is calculated. The system control unit 5 accepts new transfer requests only when it is determined that there is no transfer request that cannot complete its data transfer within the transfer  
15 completion time. This determination is performed every time when there is a new transfer request and the system control unit 5 accepts those transfer requests when it is determined that all the data transfer of those transfer requests will complete within the transfer  
20 completion time. The accepted transfer requests are managed in queues as shown in FIG. 7. When the transfer request is not accepted, then such rejection is reported to the origin of the transfer request.

Accordingly, when such a new transfer request  
25 is accepted, each of the reading unit 1, the image-

forming unit 2, and the facsimile unit 3, which transfers the data or where the data is transferred to, can always optimally perform respective processes without substantially reducing the processing rate.

5 Therefore, high productivity of the data processing device such as an image-forming device can always be maintained.

As shown in FIG. 7, in the waiting queues, identification for identifying the transfer request, the origin of the transfer request, the current status, the amount of data to be transferred, the transfer completion time, etc., are registered in the order in which the transfer requests are accepted. Accordingly, the transfer requests are processed sequentially in the accepted order. In the waiting queues, the transfer completion time is represented as the time of the day. Every time when the current status of the transfer request changes, such as a start or completion of a data transfer, such a change in the current status is reported to the origin or the transfer request with the identification.

The processing order, which is the order in which the transfer requests are accepted, registered in the waiting queue can be re-ordered at will. Further, 25 the execution of one of the transfer requests can be

abandoned by removing such a transfer request from the waiting queue. Such removal is reported to the origin of the transfer request with the identification.

According to the first embodiment of the present  
5 invention, a plurality of waiting queues are provided,  
for example, a waiting queue for the input (data  
transfer to the storage unit 3) and a waiting queue for  
the output, in order to realize a plurality of  
input/output data transfers simultaneously.

10 It is noted that according to the first  
embodiment of the present invention, the new transfer  
requests are accepted only when it is determined that  
all the data transfer of the transfer requests will  
complete within the transfer completion time. However,  
15 it is also possible to determine a timing to start the  
data transfer on the condition that all the data  
transfer can be completed within the transfer completion  
time, and such timing may be accepted. Alternatively,  
level of importance may be taken into consideration when  
20 accepting transfer requests. That is to say, those  
transfer requests that can be cancelled may be  
eliminated from the waiting queue and those transfer  
requests that can be postponed may be processed later.

Although according to the first embodiment of  
25 the present invention, each of the reading unit 1, the

image-forming unit 2, and the facsimile unit 3 corresponds to the data processing means, the number and the types of the data processing means are not limited thereto. The present invention is applicable to the 5 data processing device implemented with a plurality of various data processing means.

Programs that realize the operation of the data processing device (image-forming device) and the variations thereof may be stored on a medium such as a 10 CD-ROM, DVD, or an optical disk and may be distributed. Alternatively, all or a part of such programs may be distributed through a transmission medium used in a public network, etc. A user may obtain and load such programs onto the existing data processing device in 15 order to apply the present invention to such a device. In this sense, the recording medium may be such that the device distributing the programs can access the medium.

A second embodiment of the present invention is described hereinafter. The configuration and the 20 operation of each part constituting the second embodiment according to the present invention is the same as that of the first embodiment according to the present invention. Therefore, the descriptions of FIG. 1 through FIG. 6 are omitted.

25 In the second embodiment of the present

invention, in addition to the configuration mentioned in FIG. 1 through FIG. 6, there are provided priority designation means for designating priority of the image signal input/output operation; input/output operation request acceptance means for accepting a plurality of image signal input/output operation requests; processing order control means for determining the processing order of the image signal input/output operation requests based on the respective priorities; interruption determination means for determining whether the current image signal input/output operation is interruptible; and interruption/resumption control means for interrupting/resuming the current image signal input/output operation based on the priority of the image signal input/output operation and the determination result from the interruption determination means. These means are provided in the system control part 5.

The priority designation means designates priority of the image signal transfer operation when the execution of the image signal input/output operation is requested. The processing operation of the priority designation means is described with reference to FIG. 8.

On receiving the execution request of image signal input/output operation, the priority designation

means receives a priority designation request from the operational unit 4 shown in FIG. 1 (S100). Then, the priority designated from the operational unit 4 is set for the image signal input/output when its execution is requested (S101). When the priority designation means does not receive the priority designation request from the operational unit 4, the priority of the image signal input/output operation is set to a default value (S102).

The priority designation means enables  
10 designating priority when executing the image signal input/output operation is requested and thus an order of priority can be determined.

A series of processing operations of the processing order control means and  
15 interruption/resumption control means is described with reference to FIG. 9.

On receiving the plurality of execution requests for image signal input/output operation (S110), the execution request with the highest priority is  
20 searched for in the execution requests (S111). Then, it is determined whether the current operation is interruptible or not (S112). When it is determined that the operation of the current image signal input/output operation request is interruptible, the priority of the  
25 current image signal input/output operation request and

the priority of the received image signal input/output operation execution request are compared (S113). When the priority of the received image signal input/output operation execution request is higher than the priority 5 of the current operation, the current operation is interrupted (S114), the received image signal input/output operation is executed (S115), and the interrupted operation is resumed when the received image signal input/output operation is completed (S116). When 10 the current operation cannot be interrupted or when the priority of the current operation is higher than the operation of the received operation, the current operation is continued.

The processing operation of the input/output 15 operation request acceptance means for accepting the plurality of image signal input/output operation requests is described with reference to FIG. 10.

It is determined whether a plurality of the received image signal input/output operation requests 20 are received or not (S120). When a plurality of requests are received, the data transfer from the primary memory device to the secondary memory device is performed in several transfers (S121). When a plurality of requests are not received, i.e. only one request is 25 received, the data transfer from the primary memory

device to the secondary memory device is performed all at once (S122). The reception of the plurality of operation requests is continually checked until the data transfer is completed (S123). Accordingly, divided data transfer enables receiving the plurality of operation requests.

By providing means for obtaining a primary memory region for storing image data, and means for obtaining a secondary memory region, in which image data 10 is compressed (converted) by the compression-decompression part 38, it is possible to obtain any capacity or fixed capacity for the respective regions. Further, in order to realize the divided data transfer, the series of processes including obtaining the fixed 15 capacity of the primary memory region; converting the image data corresponding to the fixed capacity; and transferring the converted image data to the secondary memory region is repeatedly performed.

The processing operation wherein the data in 20 the primary memory region is transferred to the secondary memory region in a single transfer is described with reference to FIG. 11.

First, a region that can hold all the amount of the image data stored in the primary memory device 25 (image memory 32), after such image data is compressed,

is reserved in the primary memory device (S130). Then,  
the image data is compressed using the compression-decompression part 38 (S131). The compressed image data  
is stored in the region reserved in the primary memory  
5 device in S130 (S132). After storage, a region for  
holding the amount of the compressed image data is  
reserved in the secondary memory device (HDD 34) (S133).  
Then, the image data in the primary memory region is  
transferred to the secondary memory region (S134).

10 After the completion of the transfer, the region  
reserved in the primary memory device is released (S135).  
The processing operation wherein the data in  
the primary memory region is transferred to the  
secondary memory region in multiple transfers is  
15 described with reference to FIG. 12.

First, a region with fixed capacity for  
holding the image data after compression is reserved in  
the primary memory device (S140). Since this region has  
fixed capacity, there is no relation with respect to the  
20 amount of the image data after compression. Then, the  
image data is compressed using the compression-decompression part 38 (S141). The compressed image data  
is stored in the region reserved in the primary memory  
in S140 (S142). At this time, all of the compressed  
25 image data may not be stored in the reserved region of

fixed capacity. Therefore, depending on a completion response of the compression-decompression part 38, it may be necessary to vary the processing operation. A region corresponding to the used capacity of the primary

5 memory region with fixed capacity is reserved in the secondary memory device (S143). Then, the image data in the first memory region is transferred to the secondary memory region (S144). After the completion of the transfer, it is determined whether the compression of

10 all image data is completed or not (S145). When it is determined that the compression of all image data is not completed, the processing operation returns to S141 to continue with the compression. The newly compressed image data is overwritten onto the region with fixed

15 capacity in the primary memory device, the previous image data stored in the primary memory region having already completed the transfer. When compression of all image data is completed, the region with fixed capacity in the primary memory device is released (S146).

20 The data transfer capability can be estimated from the data transfer rate to the secondary memory device. By selecting the amount of data conversion and the storage capacity based on the data transfer capability, it is possible to efficiently select the

25 utilization rate of the primary memory region and the

secondary memory region in the respective memory devices.

As described above, in the second embodiment according to the present invention, it is possible to reduce the processing time needed for operation requests 5 with higher priority when a plurality of image signal input/output operation requests are received by determining the processing order according to the priority designated at the time of input/output operation request; determining whether the current 10 operation is interruptible; and controlling interruption/resumption when the current operation is interruptible.

In addition, in the second embodiment according to the present invention, the determination of 15 whether the current operation is interruptible can be made from the transfer time, processing time, etc., of each image signal input/output operation. However, interruption designation means may be provided for designating whether the image signal input/output 20 operation is interruptible at the time of execution request of such image signal input/output operation, and the determination of whether the current operation is interruptible may be based on the designation information from the interruption designation means. 25 The processing operation of the interruption designation

means is shown in FIG. 13.

On receiving the execution request for the image signal input/output operation, the interruption designation means accepts designation of

5 interruptibility or non-interruptibility for the received image signal input/output transfer operation from the operational unit 4 (S150). Then, the setting of interruptibility or non-interruptibility is performed (S151). When there is no designation input from the  
10 operational unit 4, then the image signal input/output operation is set as non-interruptible (S152).

Accordingly, it is possible to designate that the current operation is interruptible or non-interruptible.

Further, it is possible to provide priority-based-processing selection means for selecting whether to perform the processing operation based on the priority such as shown in FIG. 9. The processing operation of the priority-based-processing selection means is described with reference to FIG. 14.

20 On receiving the execution request of image signal input/output operation, the priority-processing selection means accepts a priority-based-processing request from the operational unit 4 (S160). On receiving such a request for performing control based on  
25 priority from the operational unit 4, the control of

execution/interruption/resumption of the image signal input/output operation based on the priority is enabled (S161). When the priority-based-processing request is not received, then the control based on the priority is 5 disabled (S162).

Accordingly, by enabling the switching of the control based on the priority by providing such priority-based-processing selection means, it is possible to perform operations according to need.

10 It is to be noted that the first embodiment of the present invention and the second embodiment of the present invention may be combined. To state it differently, the first embodiment of the present invention in general relates to the management of accesses and thus to the management of data transfer processes in response to such accesses made by the data processing units (the image input unit/image output unit) to the memory. The data transfer processes that cannot be completed within the data transfer completion 15 time, which data transfer processes are usually requested at a later time than others, are either prevented or postponed. Accordingly, in the first embodiment of the present invention, when a plurality of data transfer processes are to be executed 20 simultaneously, at least some of the data transfer 25

processes are unable to meet the time constraint (i.e. to complete the data transfer process within the data transfer completion time), therefore such transfer processes are may be disenabled. Therefore, the 5 productivity of the device is improved by obviating generation of data transfer processes that cannot be completed within the data transfer completion time. The second embodiment of the present invention in general relates to how to select among the data transfer 10 processes in response to the accesses made by the data processing units to the memory so as to efficiently execute a plurality of operations. Here, the data transfer processes may include those data transfer processes that are to be prevented or postponed in the 15 first embodiment of the present invention. The efficiency of the device can be further improved by giving priorities to the data transfer processes so that the data transfer processes with a higher priority can be executed first and the data transfer processes with a 20 lower priority are prevented or postponed as appropriate.

Further, the present invention is not limited to these embodiments, and variations and modifications may be made without departing from the scope of the present invention.

25 The present application is based on Japanese

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priority application Nos. 2002-272402 filed on September 19, 2002, and 2002-274138 filed on September 19, 2002, the entire contents of which are hereby incorporated by reference.